CLAIMS

What is claimed is:

1. A memory cell structure, comprising:

a substrate having a bottom electrode at least partially disposed within the substrate;

a pad disposed at least partially over the substrate;

a phase change element disposed at least partially over the substrate and adjacent to the pad, the phase change element being operatively coupled to the bottom electrode; and

a top electrode operatively coupled to the phase change element.

2. The memory cell structure as set forth in claim 1, wherein the phase change element is formed on a sidewall of the pad.

3. The memory cell structure as set forth in claim 1, wherein:

the pad comprises a top surface, a bottom surface, and at least two sidewalls disposed between the top and bottom surfaces; and

the phase change element is formed on one of the at least two sidewalls of the pad.

4. The memory cell structure as set forth in claim 3, and further comprising:

another phase change element formed on another one of the at least two sidewalls of the pad; and

top and bottom electrodes operatively coupled to the other phase change element.

5. The memory cell structure as set forth in claim 4, wherein the pad is disposed between the phase change element and the other phase change element.

6. The memory cell structure as set forth in claim 1, wherein:

the bottom electrode is disposed within the substrate;

the pad is disposed over and substantially parallel to a top surface of the substrate;

the phase change element is disposed over the substrate; and

the phase change element contacts both the bottom electrode and the top electrode.

7. The memory cell structure as set forth in claim 1, wherein the phase change element has its longest dimension parallel to the substrate.

8. The memory cell structure as set forth in claim 1, wherein the pad is formed by a method comprising:

depositing a first material layer over the substrate;

etching the first material layer to form a pad strip and to expose the bottom electrode; and

etching the pad strip to form the pad.

9. The memory cell structure as set forth in claim 8, wherein the first material layer comprises a dielectric material.

10. A method of forming the phase change element of claim 1, comprising:

depositing a phase change layer over both the pad strip of claim 8 and the substrate;

etching back the phase change layer to form a phase change strip; and

etching the phase change strip to form the phase change element.

11. The method as set forth in claim 10, wherein the phase change layer comprises a chalcogenide material.

12. A memory cell, comprising:

a substrate having a bottom electrode;

a phase change element having a maximum length extending between two opposing ends and being disposed adjacent to the bottom electrode; and

a top electrode adjacent to the phase change element;

wherein the bottom electrode and the top electrode are disposed at the opposing ends of the phase change element.

13. The method as set forth in claim 12, wherein the phase change layer comprises a chalcogenide material.

14. A memory cell, comprising:

a substrate having a bottom electrode;

at least one phase change element disposed over a surface of the substrate and adjacent to the bottom electrode; and

a top electrode adjacent to the phase change element;

wherein the phase change element has its longest dimension parallel to the surface of the substrate.

15. The method as set forth in claim 14, wherein the phase change layer comprises a chalcogenide material.

16. A method of forming the at least one phase change element of claim 14, comprising:

depositing a first material layer over the substrate;

etching the first material layer to form a pad strip and to expose the bottom electrode;

depositing a phase change layer over the pad strip and the substrate;

etching back the phase change layer to form a phase change strip;

etching the phase change strip to form the phase change element; and

etching away the pad strip.

17. The method as set forth in claim 16, wherein:

the at least one phase change element comprises a plurality of phase change elements;

the etching back of the phase change layer comprises etching back the phase change layer to form a plurality of phase change strips; and

the etching of the phase change strip comprises etching the phase change strip to form a plurality of phase change elements.

18. The method as set forth in claim 16, wherein the first material layer comprises a dielectric material.

19. The method as set forth in claim 16, wherein the first material layer comprises polysilicon.

20. The method as set forth in claim 16, wherein the phase change layer comprises a chalcogenide material.